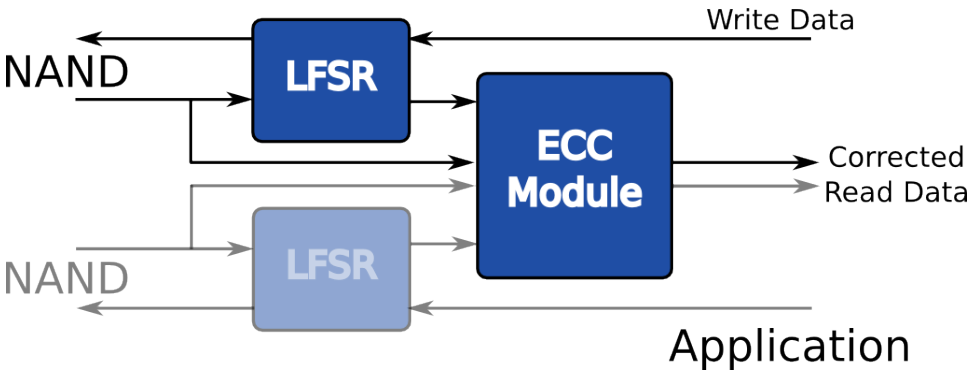
G13 BCH Verilog ECC IP

The Cyclic Design G13 BCH encoder/decoder provides error correction code (ECC) capabilities for applications such as data storage and transmission. BCH is optimal for applications where errors are non-correlated (non-burst) such as NAND flash.

The Cyclic Design G13 BCH Verilog IP is optimized for 512B correction blocks, but supports programmable block sizes from 2 to 900 bytes and correction from 2 to 16 bits per correction block. Block size and ECC level can be dynamically changed for each correction operation, allowing flexibility in the design of the application controller. Verilog RTL incorporates SystemVerilog Assertions (SVA) to perform internal property checks and validate I/O interface usage when integrated into target controller.

The control interface is optimized around a 16-bit datapath to enable applications using DDR flash devices. Optionally, an 8-bit interface can be selected via design parameters. The data interfaces utilize a ready/valid handshake to provide a simple control interface to ease integration into the application controller.



Architecture

The Cyclic Design BCH ECC IP is implemented as two separate modules: an LFSR module (which generates parity for outgoing data and syndromes for incoming data) and an ECC module that computes and applies corrections to the incoming data stream.

The LFSR module is implemented in a combined syndrome/parity LFSR in order to minimize design area. Separate parity and syndrome generation LFSRs are also available for cases where splitting the data streams simply implementation. The IP is designed to support both single-channel and multi-channel ECC configurations.

The ECC module interfaces synchronously to the LFSR, but the internal computations may be run asynchronously at a higher frequency in order to minimize latency and area required for the design. All asynchronous interfaces are manged within the IP for ease of integration. The ECC module can also be used in a FIFO-less configuration in order to maintain the existing data flow infrastructure within the controller. In this configuration, the ECC module produces a stream of correction operations which the application controller can use to apply to the incoming data stream.

Highlights:

- Verilog RTL
- 2-16 bit error correction
- 2-900 data bytes per block
- 13 parity bits required per correctable error
- Design parametrized for a wide range of area / performance options
- Pipelined correction operation supports 3 concurrent corrections
- Correction module supports an internal asynchronous mode for higher performance and decreased area
- 8 or 16-bit data path
- LFSRs support shifting of 2, 4, 8, or 16 bits per cycle.
- Chien Search supports 4, 8, or 16 corrections per cycle
- Single or Multiple-channel design
- IP can be customized to meet other design goals
- Each IP Configuration is regressed via FPGA

Performance

LFSR bandwidth and area is determined by the number of bits shifted per clock cycle. This value is parametrized and can be adjusted by the customer to 2, 4, 8, or 16 bits per cycle. The LFSR option should be selected based on the highest raw data rate required by the application.

The combined latency through the ECC module depends primarily on the block size and ECC level in use as well as the parameters used for the design. The Chien Search module supports processing at 4, 8, or 16 bits/cycle and the Berlekamp module supports several parameter to balance area and performance . The ECC module is pipelined to accommodate a 2-stage pipeline to maximize correction throughput. When used, the FIFO is typically sized to accommodate two 512B data blocks, however customer can modify the FIFO size to meet design criteria.

The design supports implementation at 200 MHz in an Altera Stratix IV class FGPA, 300+ MHz in most LP processes, and 600+ MHz in most GP processes. Contact Cyclic Design for area and performance metrics of specific configurations since these metrics vary widely by configuration.

Customization

Cyclic Design can customize the base BCH implementation to match customer needs, including custom data widths, block sizes, and ECC levels. Further customization can be done to the design to meet specific area or performance goals. Cyclic Design can also create custom multi-channel ECC configurations to provide resource sharing of an ECC module between multiple channels.

Cyclic Design can also create customized BCH solutions for other applications that require different correction block sizes or ECC levels. Visit http://cyclicdesign.com/index.php/products for more information on the other IP cores below:

- G12 – 256B, ECC 2-16
- G13/G13X – 512B, ECC 2-16 (G13) or ECC 2-64 (G13X)
- G14/G14X – 1024B, ECC 2-40 (G14) or ECC 2-96 (G14X)
- G15 – 2048B, ECC 2-96

Deliverables

- Synthesizable Verilog RTL design
- Verilog testbench and C models
- Design Documentation

Purchase of the IP includes consulting time required to configure and deliver the customer's selected configuration as well as integration support for one year. Any changes to the internal design to meet customer RTL requirements (rule checks, mapping to RAMS, etc) is included in the IP license cost. Changes to the control interfaces or modification to the block functionality must be negotiated at license time or through a consulting agreement.

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